ÜberNIC Half-Height Ethernet Adapters

LMS
THE POWER OF THE POSSIBLE

784ns	910ns	20.45ns	99.8%
Minimum Latency	99th Pctl. Latency	99th Pctl. Latency Std. Dev.	2.5Gbps Latency <=949ns

Full Stack I/O Latency: 10GbE; 5,000,000 64B TCP Frames From 0.1 - 10Gbps To/From User-Space via PCIe Gen 5 w/ÜberLoad

Uncompromising Foundation

Every ÜberNIC utilizes the same architecture - hardware network stack, no compromise on latency or reliability. Both products are fully programmable via the ÜberFPGA FDK, enabling network-edge logic, message preprocessing, and custom workload offload. The difference is in platform, density, and connectivity range.

ÜberNIC ML

Ultra-Low-Latency Programmable SmartNIC

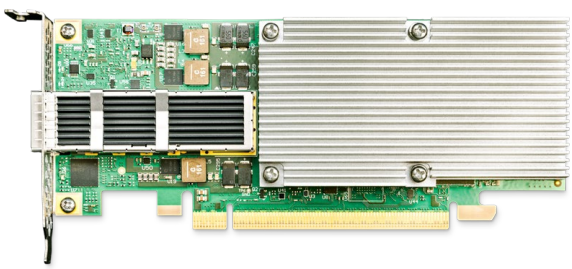
- ÜberFPGA FDK For Seamless Upgrades
- AMD FPGA Ecosystem
- 2 DSFP28, 4 x 1/10/25GbE Interfaces
- 19W Total Draw
- Full Line Rate, Sub-µs, No Drops

Board Manufacturer: AMD

ÜberNIC Ultra+

High-Density Programmable SmartNIC

- Hyperscale Throughput 1GbE to 400GbE
- Altera FPGA Ecosystem
- 1 QSFPDD, 8 x 1/10/25GbE Interfaces
- 54W Total Draw
- Full Line Rate, Sub-µs, No Drops



Board Manufacturer: Molex

ÜberNIC IP Suite

Base IP

- ÜberStack
- ÜberL2
- ÜberLoad
- ÜberSock

Add-On IP (HW Logic)

- ÜberFPGA FDK (Aug. ‘26)
- ÜberPTM
- ÜberPTP
- ÜberWR
- ÜberCAP
- ÜberDPI (Oct. ‘26)
- ÜberRAW (Aug. ‘26)
- NIC… to NAC…

LMS Partners Include

intel · altera An Intel Company · AMD · Red Hat · Bittware a molex company · AM·BROTOS · HAMBURGNET High Performance IT - Storage, Server, Networks & Consulting · JABIL · DELL · CERN · blackcore technologies

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	ÜberNIC Ultra+	ÜberNIC ML
PLATFORM		
FORM FACTOR	Single-Slot, HH x HL	Single-Slot, HH x HL
FPGA	Altera AGI-023	AMD VU23
NETWORK STACK	Hardware	Hardware
NETWORK I/O		
CAGE(S)	1 x QSFPDD	2xDSFP28
MAX INTERFACES	8	4
LINK SPEEDS	1/10/25/40/50/100/200/400 GbE	1/10/25 GbE
TRANSCEIVER SPEED (ONE-WAY)	72.5ns	21.0ns
FPGA		
LOGIC ELEMENTS	2.308M	2.252M
BLOCK RAM	204Mb	79Mb
ULTRA RAM / eSRAM	18Mb	99Mb
MEMORY		
DDR4	16GB	8GB
PCIE		
NATIVE VERSION	5	4
SUPPORTED VERSION(S)	5/4/3	4/3
LANES	16	8
CXL 1.1 & 2.0 (ON REQUEST)	Y	N
AMD SDCI	Y	Y
POWER		
8 INTERFACES (UNIT/INTERFACE)	54W/6.7W	N/A
4 INTERFACES (UNIT/INTERFACE)	34W/8.5W	19W/4.7W
PRECISION TIME		
OSCILLATOR	TCXO	TCXO
PTP IN HOST (LinuxPTP)	Y	Y
PTP IN FPGA (ÜberPTP)	Y	Y
WHITE RABBIT IN FPGA (ÜberWR)	Y	Y
TIMESTAMPING IN FPGA (ÜberTime)	Y	Y
PTM (PRECISION TIME MEASUREMENT)	Y	N
OPERATING SYSTEM		
RED HAT/FEDORA/ALMALINUX	Y	Y
UBUNTU	Y	Y
DEBIAN	Y	Y
SUSE	Y	Y